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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,537	03/12/2004	Li-Kong Wang	728-228 CON (YOR9-2002-00)	7838
28249	7590	03/29/2005	EXAMINER	
DILWORTH & BARRESE, LLP 333 EARLE OVINGTON BLVD. UNIONDALE, NY 11553			CUNNINGHAM, TERRY D	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/799,537

Applicant(s)

WANG ET AL.

Examiner

Terry D. Cunningham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>10/06/04</u> | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification fails to adequately describe the circuit of Fig. 4. The operation for the circuit of Fig. 4 is discussed in lines 4-20 of page 8, however this discussion is not consistent with what would be understood by one skilled in the art. This section firstly states that transistor F3 is “preferably an nFET”. This section goes on to state that “[w]hen either of PCS(x) and CES(x) are ‘low’, CS(x) switches FET F3 ‘off’ so that no DC current flows to the regulator system 412”. This statement is not understood. Firstly, when “either PCS(x) and CES(x) are ‘low’”, the output of NAND gate G1 will be high, which causes nFET transistor F3 to turn on. With transistor F3 on, node V_I will be grounded. Since V_I will be grounded, it appears that the second part of the statement is correct. Thus, it appears that “off” in line 11 should be changed to --on--. Additionally, this section states that “[w]hen both PCS(x) and CES(x) are ‘high’, CS(x) switches FET F3 ‘on’ and power supply voltage V_H is provided to the regulator system 412” Again, this language is not understood. Firstly, contrary to the language, when “both PCS(x) and CES(x) are ‘high’” the output of NAND gate G1 will necessarily be low, causing

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nFET transistor F3 to turn off. Therefore, it appears that “on” in line 13 be changed to --off--. Further, the language stating that “ V_H is provided to the regulator system 412” is not consistent with what would be understood. As would be understood, a voltage having a level equal to V_H less the threshold drops of pFET transistors F1 and F2 will be provided to system 412, contrary to that stated.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 11-12, there is no support found in the specification for the statement that “the pump control signal being based on the clock control signal”. Contrarily, the specification provides that the “pump control signal” is “in accordance with”, i.e., based on, voltage V_H and diodes F1 and F2, not the “control signal” CES. As seen, the “clock control signal” only enables and disables V_I .

Claims 2-12 and 21 are rejected for the reasons discussed above with claim 1.

Examiner has fully considered Applicant’s remarks for the above rejection and has not found them to be persuasive. Applicant again traverses the rejection and requests clarification. The specification expressly states that nFET F3 “switches the regulator system 412 on or off”, whereas claim 1 states that “pump control voltage” BC, which controls “a pump systems” (discussed in lines 1-5 of page 9 of the specification). As disclosed, “pump control voltage” BC is a regulated analog voltage signal that has a level based on the level of the voltage V_I . This

voltage level is clear not base on signal CES. It is suggested that “based on” in lines 12-13 should be changed to --enabled and disabled in response to--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. §102(b) as being anticipated by Mullarkey (USPN 6,005,812).

With respect to claims 1-12 and 21, Mullarkey discloses, in Figs. 1 and 3, a circuit comprising: “a plurality of local DC voltage generators (see Col. 5, lines 6-11, which state that each device can include a DRAM device 10, as in Fig. 1)”, each having “a regulator system (14 and 24)” “receiving a clock signal (CLK) and outputting one pump control signal (REG-DIS*) and “a pump system (16 and 18)” and a “respective control signal (TEST)”, all connected and operating similarly as recited by Applicant.

With respect to claims 13-20, clearly the above circuit to Mullarkey will provide a method comprising: “distributing a plurality of local DC voltage generator throughout the chip (see Col. 5, lines 6-11, which state that each device can include a DRAM device 10, as in Fig. 1)”; “supplying a clock control signal (with 16)”; “generating, in a section (14)..., a pump control signal (REG-DIS*)”; “receiving, with a pump system (18)”; and “supplying the DC voltage (as Vccp at node 12)”.

Examiner has fully considered Applicant’s remarks for the above rejection and has not found them to be persuasive. Applicant remarks, “No single integrated circuit or chip in

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Mullarkey contains more than one voltage generator“. However, the claims do not recite “a single integrated circuit”. Further, Examiner contends that it would have been reasonable to consider two integrated circuits as being an “integrated circuit”. In Addition, it appears that Applicant is too narrowly interpreting the phrase “integrated circuit”. It is notoriously well known that the term “integrated” merely means together. Clearly, the circuit arrangement of Mullarkey is “together”. Therefore, giving the phrase “integrated circuit” its broadest reasonable interpretation, the reference to Mullarkey would meet the claim language. Thus, this rejection is hereby maintained.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 703-308-4872. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is 703-308-0956.

TC
March 23, 2005


Terry D. Cunningham
Primary Examiner
Art Unit 2816